Application No. 09/346,361

REMARKS

The above identified patent application has been amended and reconsideration and reexamination are hereby requested.

The Examiner has indicated that he would entertain treating corrected claims 15-19 and 24 to the elected invention if the dependency is corrected. The Applicants has amended claims 15 - 19 to correct their dependencies to be dependent on the elected invention. Claim 24 is dependent on corrected claim 17.

The Examiner has suggested that Applicants cancel non-elected claims 1-3 and 7-10. The Applicants have canceled non-elected claims 1 - 3 and 7 - 10 to pursue them in a divisional application.

The Examiner has objected to an informality in line 8 of claim 14 with regard to the misspelling of the word noise. The Applicants have amended claim 14 to correct the misspelling.

The Examiner has rejected claim 27 under 35 U.S.C. 112, second paragraph, as being indefinite in that there is no antecedent basis for many elements of the claim. The Examiner suggests that this claim should depend from claim 26. The Applicants have amended the dependency of claim 27 as suggested by the Examiner.

The Examiner has rejected claims 4-6, 11-13 and 26 under 35 U.S.C. 102(b) as being anticipated by Adrian or Howatt. The Examiner has also rejected claims 14, 20, and 25 under 35 U.S.C. 102(e) as being anticipated by Tripathi et al. The Examiner has further rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over Tripathi et al. in view of Adrian et al.

Applicants have amended Claim 4 to call for (underlining added for emphasis) ... A <u>semiconductor</u> H-bridge controller ... .

As such, Applicants submit that Claim 4 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b).

The present invention provides for a <u>semiconductor</u> implementation of the power output stage of an H-bridge controller configured to create a three state condition.

Adrian et al. on the other hand provides a broad disclosure of a "tri-state power switch drive logic stage" (28 of fig. 8a), that drives the "power switches" (26 of fig. 8a). The construction of the switches are disclosed as nothing more than <u>common electro-mechanical switches</u>.

Likewise, Howatt provides for nothing more than an <u>electro-mechanical switch</u> in the disclosed "switching arrangement" (column 5, line 15) and (26 figs. 3) and (26 fig 7).

Accordingly, Applicants submit that Claim 4 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b).

Claim 5 and 12 dependent on Claim 4. As such, Claims 5 and 12 are believed allowable based upon Claim 4.

Applicants have amended Claim 6 to call for (underlining added for emphasis) ... A digital amplifier comprising .... a <u>semiconductor</u> H-bridge controller ... .

As such, Applicants submit that Claim 6 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b) for the same reasons as discussed above with regard to claim 4.

Claim 13 is dependent on Claim 6. As such, Claim 13 is believed allowable based upon Claim 6.

Applicants have amended Claim 11 to call for (underlining added for emphasis) ... a digital amplifier comprising a <u>semiconductor</u> H-bridge controller which generates a multi-state output.

As such, Applicants submit that Claim 11 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b) for the same reasons as discussed above with regard to claim 4.

Applicants have amended Claim 26 to call for (underlining added for emphasis) ... a digital amplifier comprising a <u>semiconductor</u> H-bridge controller which generates a multi-state output.

As such, Applicants submit that Claim 26 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b) for the same reasons as discussed above with regard to claim 4.

Claim 27 is dependent on Claim 26. As such, Claim 27 is believed allowable based upon Claim 26.

Applicants have amended Claim 14 to call for (underlining added for emphasis) ... a sampling stage with an input connected to the output of the noise shaping network, and generating a sampled signal, the sampling stage having a predetermined sampling frequency, and <u>generating an output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple</u> ... a feedback loop providing the output of the sampling stage <u>coupled directly</u> to the summation circuit.

As such, Applicants submit that Claim 14 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b).

The present invention provides for a sampling frequency that has <u>particular characteristics</u>. The sampling frequency is <u>selected to generate an output signal from the sampling stage with a lower transition rate with respect to the sampling frequency by a predetermined multiple</u>.

Tripathi et al. on the other hand merely discloses <u>a sampling stage operating at an unspecified sampling frequency</u>. The <u>selection of the sampling frequency is not disclosed</u>, its presence is only identified (column4, line 66) (column 5, line 59) (column 6, line 19) (column 6, line 29).

Accordingly, Applicants submit that Claim 14 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b).

Claims 15-19, 21-25 are dependent on Claim 14. As such, these dependent claims are believed allowable based upon Claim 14.

Applicants have amended Claim 20 to call for (underlining added for emphasis) ... a sampling stage with an input connected to the output of the noise shaping network, and <u>generating an output signal</u> with a multi-state output, <u>with an least three states</u> ... a feedback loop providing the output of the sampling stage <u>coupled directly</u> to the summation circuit.

As such, Applicants submit that Claim 20 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b).

The present invention provides for a sampling stage with a multi-state output of at least 3 output states. In addition, the feedback loop is coupled directly to the summation circuit without any additional circuitry coupled between those nodes.

Tripathi et al. on the other hand merely discloses a generic clocked comparator clocked at a sampling rate. The particular type of the comparator utilized is not disclosed. The signal output from the comparator is only disclosed to be a logic signal, without disclosure of the type of comparator needed to provide for the characteristics of the logic signal (column 5, lines 58 to column 5 line 2). In addition, Tripathi et al does not disclose feedback coupled directly to the summation circuit. The feedback is indirectly coupled through D/A circuit 418 of figure 4b.

Accordingly, Applicants submit that Claim 20 is not anticipated by Adrian et al. or Howatt under 35 U.S.C. §102(b).

Therefore, in view of the above amendment and remarks it is submitted that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show amendments made**."

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By Richard J. Paulan

Richard J. Paciulan
Reg. No. 28,248
626/795-9900

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VERSION WITH MARKINGS TO SHOW AMENDMENTS MADE

Claims 4-6, 11-21 and 26-27 have been amended as follows (Underlinings indicate insertions; brackets indicate deletions.):

4. (amended) A <u>semiconductor</u> H-bridge controller wherein its outputs consist of three states.

5. (amended) A <u>semiconductor</u> H-bridge controller of Claim 4 wherein the gating mechanism for each leg is independently controlled.

6. (amended) A digital amplifier comprising:

a modulation stage for signal shaping; and

a <u>semiconductor</u> H-bridge controller wherein its outputs consist of three states.

11. (amended) A digital amplifier comprising:

a modulation stage for signal shaping; and

[an] <u>a semiconductor</u> H-bridge controller which generates a multi-state output.

12. (amended) The digital amplifier of claim 5, wherein the <u>semiconductor</u> H-bridge controller a multi-state output, includes at least three states.

13. (amended) The digital amplifier of claim 6, wherein the <u>semiconductor</u> H-bridge controller has two output terminals, and the output signal on each terminal is independently controlled.

14. (amended) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to the output of the summation circuit and generating a noise shaped signal;

a sampling stage with an input connected to the output of the [nosie] noise shaping network, and generating a sampled signal, the sampling stage having a predetermined sampling frequency, and generating an output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple;

a feedback loop providing the output of the sampling stage coupled directly to the summation circuit [and the noise shaping circuit]; and

an output stage with inputs connected to the output of the sampling stage and generating an output signal.

15. (amended) The digital amplifier of claim [8] 14, wherein the output stage includes an H-bridge controller.

16. (amended) The digital amplifier of claim [8] 14, wherein the sampling [circuit] stage further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

17. (amended) The digital amplifier of claim [10] 16, wherein the logic circuit further includes a transition detector for detecting a transition in the output signal.

18. (amended) The digital amplifier of claim [8] 14, wherein the output signal of the sampling stage has a multi-state output, with at least three states.

19. (amended) The digital amplifier of claim [8] <u>14</u>, wherein the noise shaping network comprises a plurality of integrator stages.

20. (amended) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to the output of the summation circuit and generating a noise shaped signal;

a sampling stage with an input connected to the output of the noise shaping network, and generating an output signal with a multi-state output, with an least three states;

a feedback loop providing the output of the sampling stage <u>coupled directly</u> to the summation circuit [and the noise shaping circuit]; and

an output stage with inputs connected to the output of the sampling stage and generating an output signal.

21. (amended) The digital amplifier of claim 14, wherein the output stage includes [an] <u>a semiconductor</u> H-bridge controller.

26. (amended) [An] <u>A semiconductor</u> H-bridge controller which generates a multi-state output, with at least three states.

27. (amended) The <u>semiconductor</u> H-bridge controller of claim [20] <u>26</u>, wherein the <u>semiconductor</u> H-bridge controller has two output terminals, and the output signal on each terminal is independently controlled.